SAROSH

+91-7376705550 · sarosh@chargeinmotion.dev · linkedin.com/in/sarosh-chargeinmotion · github.com/ChargeInMotion · Bengaluru · Open to Remote

SUMMARY

EDA-automation engineer moving into **DFT**, with a **physical-design** foundation. 1.5 years at Elbrus Labs writing **Python**, **Bash** and **TCL** to automate IC-layout, routing and netlist work: **GDSII** tooling on **gdspy**, a **node-migration** tool that ports **standard cells** and **metal layers** down **technology nodes**, a **latchup-detection** checker, **SPICE** .cir parsers, and **Tkinter/GTK** tools the layout team used daily. Now focused on **Design-for-Test**: I built a **scan-chain simulator**, a **stuck-at fault simulator** (100% coverage on its test set), and a synthesizable **Verilog scan chain** with a **self-checking testbench**, covering **scan insertion**, **ATPG** and **fault modeling**. Strong in **Python automation**, **Linux** and scripting-heavy **EDA flows**. Available immediately.

WORK EXPERIENCE

Trainee Engineer - EDA & Layout Automation · *Elbrus Labs Pvt. Ltd., Noida* Oct 2021 – Jan 2023

- **Developed Python / gdspy tools to** automate **GDSII** layout edits and **routing of layer connections** - add, delete, resize, copy, move and **remap layers**, **metals**, labels and **cells** across large IC layouts; merge, overlap and **slice** GDS geometry by layer and **datatype**.
- **Built a node-migration tool that** converts **standard cells** and **metal layers** from a higher **technology node** to a lower one as needed (applied on a **12nm** standard-cell library): parses the foundry **layer map** (name / number / datatype / width / spacing), **slices routing-layer polygons**, **remaps layers**, and merges connected geometry.
- **Designed a latchup-detection tool** that analyses **layout geometry** to flag regions vulnerable to **latchup**, moving the check earlier than manual review.
- **Parsed transistor-level SPICE .cir netlists** with **Bash**, **awk** and **sed** to report per-instance geometry, **pmos/nmos** gate and fin counts, IN/OUT pins, and the full **cell hierarchy**.
- **Built Tkinter and GTK3 desktop tools** the layout team used daily: **Cadence Virtuoso** project/DOE launchers, a project-and-trainee status dashboard with **matplotlib** charts, and a **GDSII** inspection GUI for hierarchy, layers, datatypes, labels and instances.

TECHNICAL SKILLS

Programming: Python · C · C++ · Verilog · SystemVerilog (basics) · Perl (basics)
Python libraries: gdspy · Tkinter · PyGObject / GTK · NumPy · Pandas · Matplotlib
Scripting & Shell: Bash / Shell · TCL / Tk · Regex (grep, sed, awk) · Makefile
DFT: Scan chains · Scan insertion · Stuck-at fault models · Fault simulation · Fault coverage · ATPG (Automatic Test Pattern Generation) | JTAG / IEEE 1149.1 boundary scan, BIST (Built-In Self-Test) / MBIST (Memory BIST), Tessent / TetraMAX (studying)
Physical Design: Floorplan · Placement · CTS · Routing · STA · SPICE · Liberty (.lib) · RTL-to-GDSII
EDA Tools: Cadence Virtuoso · Cadence Encounter · Xilinx Vivado / ISE · Synopsys (learning) · Git · KiCAD
Platforms: Linux (Arch / Debian) · Docker · Raspberry Pi · Arduino / ESP32

PROJECTS

DFT Portfolio - *Python · Scan chains · ATPG · Fault simulation · Verilog* github.com/ChargeInMotion/dft-fundamentals

- **Built a scan-chain simulator** modelling N **scan flip-flops** with the three scan operations - **shift-in**, **capture** and **shift-out** - each flop a 2:1 mux selected by **scan-enable**; cross-checked against a structural **Verilog scan chain**.
- **Wrote a stuck-at (SA0 / SA1) fault simulator** that **sensitises** each fault, **propagates** it to a primary output, computes **fault coverage** (100% on the demo circuit), and derives the **minimal test-pattern set**.
- **Implemented synthesizable Verilog** (D-FF, scan-FF, 4-bit **scan chain**) with a **self-checking testbench** verified on **Icarus Verilog** - the **RTL** reproduces the Python model bit-for-bit.

Liberty (.lib) Cell Report Generator - *Bash · awk · sed · Linux · HTML · MSMTP · PD .lib files* github.com/ChargeInMotion/liberty-cell-report-generator

- **Parses Liberty (.lib) standard-cell** libraries and lists every cell by category (INV / AND / NAND / NOR / XOR / MUX / AOI / OAI / adder / latch / flip-flop / clock-gate) with its **drive strengths**.

- **Extracts a cell's timing arcs**, **internal and leakage power**, area, **operating conditions**, rail and pin information - pulling values straight out of the .lib timing **look-up tables** with **awk** and **sed**.
- **Supports best-case / worst-case corners** (fast.lib / slow.lib) and generates a formatted **HTML report** in the background while the user works in the terminal, then emails it from the shell via **msmtp** with input validation.

8-bit Breadboard Computer - *60+ 74LS ICs · EEPROM microcode · SAP-1 · KiCAD PCB* · Best Paper (team), NCRTEE 2020
github.com/ChargeInMotion/8bit-breadboard-computer

- **Built a working 8-bit CPU** (**SAP-1** architecture, after Ben Eater) from 60+ discrete **74LS** ICs and **EEPROM microcode** - clock, **ALU**, registers, RAM, **program counter** and 7-segment output - from breadboard to soldered **PCB**.
- **Flashed the microcode and program bytes** onto **28C16 EEPROMs** using an **ESP32** as the programmer; ran **fetch-decode-execute** demos (LDA / ADD / OUT).
- **Debugged the 555 clock** producing ragged edges - traced it to **IR drop** across the breadboard power rails and fixed it with rail **decoupling capacitors**.

Homelab - ChargeInMotion - *Raspberry Pi · Docker · Cloudflare Tunnel · Authelia · Pi-hole*
github.com/ChargeInMotion/ChargeInMotion-HomeLab

- **Self-hosts 18+ Docker services** on a **UPS-backed** Raspberry Pi behind a **Cloudflare Tunnel** (no open ports) and **Authelia** SSO, with recursive DNS (**Pi-hole + Unbound**) and a three-tier **backup pipeline**.

TRAINING & EDUCATION

Self-Directed DFT Study - scan insertion, ATPG, fault modeling, JTAG/BIST; hands-on Python and Verilog labs (github.com/ChargeInMotion/dft-fundamentals). Formal certification (VLSIGuru / Maven Silicon) planned. 2026

ASIC Physical Design - PinE Training Academy - floorplanning, placement, power planning, CTS, routing, STA; Bash/TCL/Python scripting for PD automation. Jul 2019 – Sep 2020

Digital Design with Verilog & Schematics - PinE Training Academy - RTL design of flip-flops, MUX/DMUX, adders and dividers; schematic entry; Xilinx ISE / Vivado implementation. Jun – Jul 2018

B.Tech, Electronics & Communication Engineering - Inderprastha Engineering College, AKTU. Technical Head, E-Yantra Robotics; NCC 'B' - Alpha Grade Certificate. 2016 – 2020

INTERNSHIPS

Intern - VLSI & Digital Design · *Aujus Technology Pvt. Ltd., Noida* Jun – Jul 2018

- **Verilog design and FPGA implementation** on **Xilinx ISE and Vivado**: calculator, LED pattern generator, seven-segment display, digital clock and stopwatch on **FPGA** hardware.

Intern - Embedded Systems · *Tantech Solutions Pvt. Ltd., New Delhi* Jun – Jul 2019

- **Built a wearable patient monitor** (SpO_2, heart rate, ECG) streaming live data to clinicians over a **Raspberry Pi 4**, plus a smart medical-bed prototype reporting body parameters to a remote server.

ACHIEVEMENTS & COMMUNITY

- **Conducted a hands-on workshop series** on **robotics and embedded systems** for 30+ junior students as Technical Head, E-Yantra Robotics - **microcontrollers** (**Arduino / 8051**), electronic components, **C programming**, **Proteus** simulation and serial communication.
- **Extra-curricular -** 3× National Gymnastics Medallist (SGFI); Gold Medal, AKTU 400m Athletics; 2nd place, college line-follower robot race; calisthenics coach and managerial-team admin at **Azad Runs** (a fitness community).
- **Community - Volunteer at** Bhartiya Janhit Kalyan Samiti (NGO) since 2014 - lead end-to-end event planning, management and execution (on/off-stage coordination and media handling) with a self-built team, and run annual food-distribution and education drives for the community.